CSC523 Homework 1
(3)(5)(8)(2)

NAME:

1. (8 pts) Consider a memory system with a level 1 cache of 32KB and DRAM of 512MB with the processor operating at 1GHz. The latency to L1 cache is one cycle and the latency to DRAM is 100 cycles. In each memory cycle, the processor fetches four words (cache line size is four words). What is the peak achievable performance of a dot product of two vectors?

Note: where necessary, assume an optimal cache placement policy.

```c
/* dot product loop */
for (i=0; i<dim; i++)
    dot_prod += a[i] * b[i];
```

2. (8 pts) As a simple model of a bus-based multiprocessor system without caching, suppose that one instruction in every four references memory, and that a memory reference occupies the bus for an entire instruction time. If the bus is busy, the requesting CPU is put into a FIFO queue. How much faster will a 64-CPU system run than a 1-CPU system?
3. (15 pts) Consider a 16x16 2-D wraparound mesh network and compute the following:

(a) network diameter

(b) bisection bandwidth (a bandwidth of each link is 200Mbits/s)

(c) bandwidth for each node
4. (8 pts) Suppose that the wire between switch 2A and switch 3B in the omega network (see Figure below) breaks. Who is cut off from whom?

5. (8 pts) Given a balanced binary tree as shown in Figure 4.7, describe a procedure to perform all-to-all broadcast that takes time \((t_s + t_w mp/2)\log p\) for \(m\)-word messages on \(p\) nodes. Assume that only the leaves of the tree contain nodes, and that an exchange of two \(m\)-word messages between any two nodes connected by bidirectional channels takes time \(t_s + t_w mk\) if the communication channel (or a part of it) is shared by \(k\) simultaneous messages.